

Submicron structures of the charge-density-wave conductor NbSe₃

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Abstract

We have lithographically patterned small wire structures into a 0.35 μm thin crystal of the charge-density-wave (CDW) conductor NbSe₃. Voltage-probe spacings down to 0.5 μm have been realized. Electrical transport measurements show that the electron-beam patterning process has not degraded the NbSe₃ material of the structures. Both the resistivity and the threshold field for CDW sliding agree with reported data on thin unpatterned crystals. The wire structures permit the study of mesoscopic CDW transport. At the shortest length scales, first observations show a reduction of the phase-slip voltage and, below 50 K, strong fluctuations and hysteresis effects in the current-voltage characteristics.

Keywords: charge-density waves, transport measurements

1. Introduction

Many bulk properties of charge-density waves (CDWs) [1] can be qualitatively understood within the Fukuyama-Lee-Rice (FLR) model [2]. This model treats the CDW as an elastic medium, moving in a random potential landscape caused by impurities. The FLR phase-coherence length is the length over which the phase of the CDW is constant. In the mesoscopic regime, sample dimensions are smaller than or comparable to this length scale, which for common CDW materials is believed to be of the order of 1 μm along the CDW chains. Whereas bulk CDW properties have been extensively studied for the last few decades, the mesoscopic regime has only recently become of interest from both an experimental [3–4] and theoretical [5] point of view.

Several routes exist for the realization of mesoscopic CDW samples. For the blue bronze Rb_{0.30}MoO₃, a thin-film technology has been developed [6]. Micron-sized wires are lithographically patterned into the films. Contact to the wires is made by electron-beam lithography, allowing CDW transport measurements on a submicron length scale. Also, the patterning of single NbSe₃ crystals has recently been

reported [7]. Periodic antidot arrays with submicron dimensions were etched into the crystals by use of electron-beam lithography. The geometry of the arrays was chosen such that normal-to-CDW electron conversion must take place within the arrays. The measurements suggest that current conversion in the antidot arrays is different from bulk samples and occurs at a length scale of 10–20 nm.

On the basis of the latter technology, we have fabricated eight-terminal submicron wire structures of NbSe₃. The structures, consisting of a thin wire with attached current and voltage leads, permit the study of CDW transport on a submicron length scale. Here we describe the fabrication of these devices, as well as a characterization of their electrical transport properties. Our data are found to be consistent with the measurements on the antidot arrays.

2. Patterning of NbSe₃ crystals

Lithographic techniques are used for the patterning and contacting of single NbSe₃ crystals. By use of electron-beam lithography, a pattern is etched into the crystal. Then, gold contacts are defined by near-UV optical lithography. The crystal thickness determines the resolution that can be obtained in the patterning process. Therefore, a thin crystal (thickness 0.35 μm) is carefully selected from a growth of NbSe₃ whiskers. The width, 27 μm , is along the *c* crystallographic axis, and the length, along *b*, is about 4 mm.

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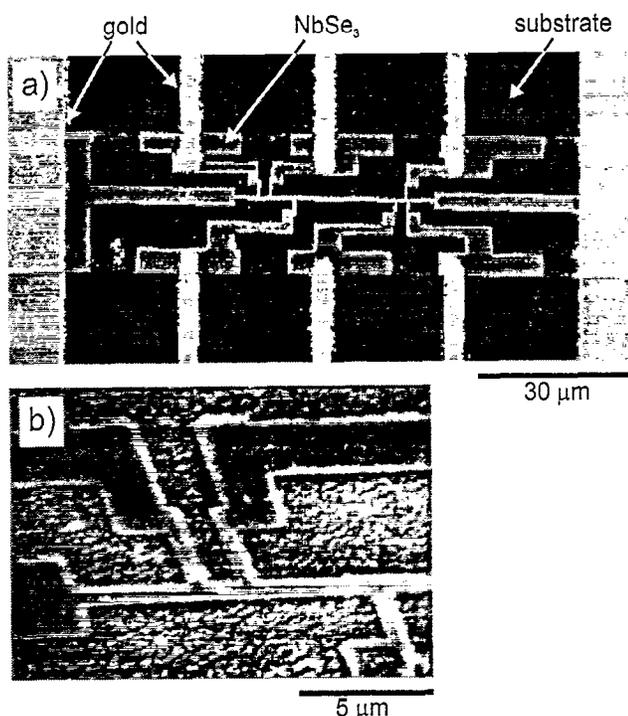


Figure 1: (a) SEM image of a $0.5 \mu\text{m}$ wide wire with current pads and voltage probes, patterned into a NbSe_3 crystal. The distances between the mids of the voltage probes from left to right are 2, 5, 20, 2, and $0.5 \mu\text{m}$. The total distance between the current pads is $100 \mu\text{m}$. Gold contact strips connect the structure to the measurement set-up. (b) Tilted-SEM image of the left part of the wire, with the $2 \mu\text{m}$ spaced voltage probes.

The crystal is glued onto a sapphire substrate using a dilute organic resist. After baking at 160°C for 5 minutes, the residues of this resist are removed in an oxygen plasma.

Lithographic patterning is achieved by direct writing with a Cambridge S240 scanning-electron microscope (SEM). To avoid charging of the substrate during exposure, first a 25 nm layer of Si is evaporated. Subsequently, a high-resolution three-layer resist sandwich is applied, consisting of $0.8 \mu\text{m}$ PMMA, then 40 nm Si, and a top layer of $0.1 \mu\text{m}$ PMMA. After exposure and development of the top PMMA layer, the middle Si layer is etched in an SF_6 plasma. Oxygen plasma etching of the bottom PMMA layer completes the patterning of the resist.

Evaporation of a 50 nm Al layer provides the mask for the etching of NbSe_3 . Lift-off of this Al layer is obtained by dissolving the resist in 2-ethoxyethyl acetate. The crystal is now etched in an SF_6 plasma. Inspection with SEM in backscattering mode shows that after six minutes the etching is complete. Then, the Al mask is etched away using Microposit MF-319 photodeveloper. Finally, the remaining Si coating is removed by SF_6 plasma etching for 10 seconds.

Gold contacts to the NbSe_3 structure are made by use of near-UV photolithography. An important issue in the fabrication process is the step coverage of the gold contacts over the crystal edge. Therefore, a thick Au layer ($0.4 \mu\text{m}$) is evaporated, partly under an angle of 45° . A $1.2 \mu\text{m}$ SR1813

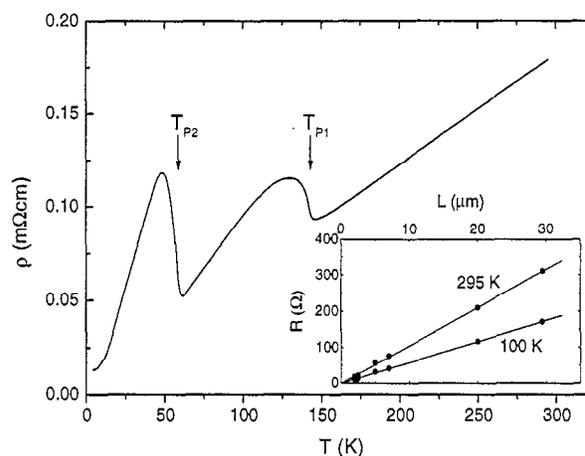


Figure 2: Resistivity versus temperature for the $0.5 \mu\text{m}$ wide wire. Voltage probes are $2 \mu\text{m}$ apart. The inset shows the scaling of the resistance with contact spacing L for two different temperatures.

photoresist layer is then spun onto the sample and baked for 30 minutes at 90°C . Alignment and exposure are done with a Karl Suzu aligner. After development of the resist, the gold layer is wet-etched in a KI/I_2 solution during 8 minutes. To avoid the use of acetone, which would dissolve the glue between crystal and substrate, the remaining resist on top of the gold contacts is then removed by further near-UV exposure and development.

Figure 1 shows one of the six eight-terminal devices that were patterned into a NbSe_3 crystal. It consists of a $0.5 \mu\text{m}$ wide wire, six NbSe_3 voltage probes at different spacings, and two large current pads. The gold contacts connect the device to the measurement set-up. Note that, instead of putting gold contacts directly on top of the wire, we have patterned voltage probes into the crystal. This lay-out has two advantages. First, no high-resolution patterning process is needed for the fabrication of the gold contacts, since contact is made to $20 \mu\text{m}$ wide voltage pads. Second, the voltage probes can be considered as nonperturbing because of the higher resistivity along the c axis of NbSe_3 .

3. Electrical transport

Electrical transport measurements have been performed on the sample of Fig. 1, and on a similar structure with a $1 \mu\text{m}$ wide wire. By using different combinations of voltage probes, measurements could be performed at several distances.

3.1 Low-bias resistivity

At small currents, the CDW is pinned. We have measured the low-bias resistivity in a four-terminal configuration by use of standard lock-in techniques. Figure 2 shows the resistivity as a function of temperature for the $0.5 \mu\text{m}$ wire. Two strong anomalies are observed, indicating the two Peierls transitions. The corresponding transition temperatures T_{P1} and T_{P2} are commonly determined by plotting $d \ln(\rho)/dT$ versus T and finding the minima in this curve. For the data of Fig. 2, this procedure yields $T_{P1}=142 \text{ K}$ and $T_{P2}=58 \text{ K}$, in agreement with the values $T_{P1}=145 \text{ K}$ and

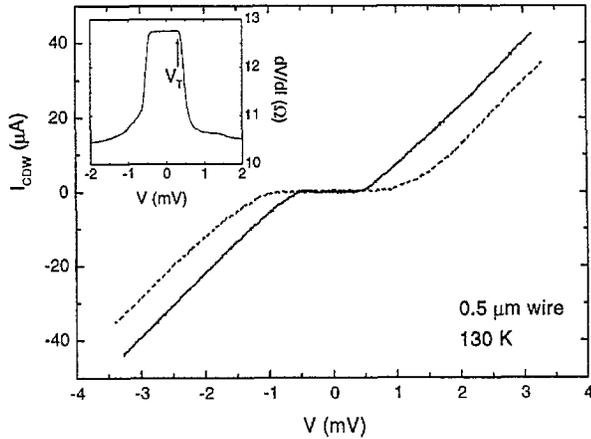


Figure 3: Charge-density wave current I_{CDW} versus voltage for the $2 \mu\text{m}$ spaced voltage contacts at 130 K. The solid line shows the curve measured in a standard four-terminal measurement, the dashed line represents the curve as measured in the transposed configuration (where current and voltage probes have been interchanged). The inset shows the corresponding differential resistance of the standard four-terminal measurement and the definition of the threshold voltage V_T .

$T_{P2}=59 \text{ K}$ that are reported in literature [1].

The inset of Fig. 2 shows the dependence of the low-bias wire resistance R on voltage-probe spacing L . As expected, the resistance scales linearly with the spacing between the voltage contacts. We have studied the resistance versus voltage-probe spacing for both wires at several temperatures. A systematic error in the length definition would result in a nonzero x -axis intersection for the $R(L)$ diagram. For the $0.5 \mu\text{m}$ wide wire we find that a systematic error, if present, must be smaller than 50 nm. This indicates that the voltage is indeed effectively measured at the middle of the probe. For the $1 \mu\text{m}$ wire, such an accurate analysis could not be performed, but these data are also consistent with the notion that the voltage contacts are nonperturbing.

The room-temperature resistivity of $0.2 \text{ m}\Omega\text{cm}$ compares well with bulk crystal values, that vary between 0.1 and $0.6 \text{ m}\Omega\text{cm}$ [8]. Furthermore, we find the same value for both wires. Apparently, the reduced lateral sample size has no implications for the low-bias resistivity. The low value for the resistivity also demonstrates that the extensive fabrication process has not significantly damaged the wires.

The data of Fig. 2 show that the wire remains metallic down to low temperatures, as is generally observed for bulk NbSe_3 crystals. Since the Fermi surface is not completely gapped at either of the two transitions, a fraction of the electrons contributes to metallic behavior even below T_{P2} . Below 10 K, the resistivity tends to saturate at a constant level. The resistance ratio $r_R = R(295\text{K})/R(5\text{K}) = 14$, independent of voltage-probe spacing. For the $1 \mu\text{m}$ wide wire, we find $r_R = 25$. These values are lower than the typical value for bulk NbSe_3 crystals. However, McCarten et al. reported that r_R depends on crystal thickness [9]. They find a strong reduction of r_R for 0.3 – $0.4 \mu\text{m}$ thin crystals, which is consistent with our measured value.

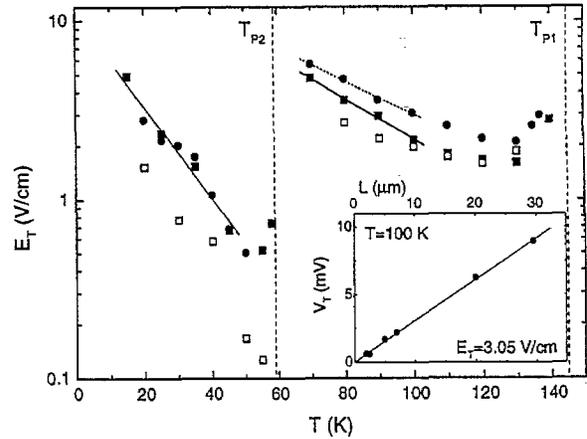


Figure 4: Threshold field E_T versus temperature for the $0.5 \mu\text{m}$ wide wire (solid circles), the $1 \mu\text{m}$ wide wire (solid squares), and an unpatterned reference crystal (open squares). The lines are fits to $E_T = E_T(0)e^{-T/T_0}$. For the high temperature region, we find $T_0=38 \text{ K}$ and $T_0=47 \text{ K}$ for the $1 \mu\text{m}$ and the $0.5 \mu\text{m}$ wide wire respectively; for the low temperature region $T_0=17 \text{ K}$ for the combined data of both wires. The inset shows the scaling of threshold voltage with voltage-probe spacing. E_T is determined as the slope of this curve.

We conclude that the measured resistivities and resistance ratios for our structures compare well with undoped crystals with the same thickness. Apparently, the patterning process has not degraded the electrical transport properties of the NbSe_3 wires, in agreement with the results obtained in [7].

3.2 Charge-density-wave sliding

We have studied the dc CDW transport by measuring $I(V)$ and $dV/dI(V)$ characteristics at various temperatures in the CDW regime. $I(V)$ characteristics are recorded by slowly sweeping the current and measuring the voltage. Simultaneously, the differential resistance dV/dI is obtained using a lock-in technique. For all voltage probe spacings and temperatures below T_{P1} , sliding of CDWs is observed. At a threshold voltage V_T the differential resistance sharply decreases, marking the transition to the sliding state.

Figure 3 shows an example of the CDW current I_{CDW} versus voltage characteristics. I_{CDW} is numerically obtained from the total current by subtracting V/R , where R is the low-bias resistance. The inset shows the corresponding dV/dI . For low bias current, the dV/dI has a constant value of 12.8Ω . Depinning occurs at the threshold voltage V_T of 0.4 mV : a sharp decrease of the differential resistance is observed, coinciding with the onset of a CDW current. For $V \gg V_T$, dV/dI stabilizes at the lower value of 10.5Ω , and I_{CDW} increases linearly with bias voltage.

The temperature dependence of the threshold field E_T has been plotted in Fig. 4. For each temperature, the threshold field has been determined from a linear fit to the plot of the threshold voltage versus probe spacing, as illustrated in the inset of Fig. 4. A comparison of E_T with data from a $0.3 \mu\text{m}$ thin unpatterned crystal (open squares) is made.

Although at low temperatures an increase of E_T is observed for the patterned structures, E_T has the same order of magnitude for both the patterned and the unpatterned crystals.

Below T_{P1} and T_{P2} , E_T show the same qualitative temperature dependence. The threshold field is high just below the transition temperature, decreases with decreasing temperature down to a minimum near $T \approx 0.8 T_P$, and then increases exponentially. In the latter region, the data can be fit using the form $E_T = E_T(0)e^{-T/T_0}$. The values for the fit parameter T_0 are denoted in the figure caption. Both the magnitude and the temperature dependence of the threshold field compare well with reported data on thin undoped NbSe₃ crystals [9].

3.3 Mesoscopic signatures

Our patterned NbSe₃ wires are very small CDW systems, in which the voltage probe spacing has, to our knowledge, for the first time been reduced to the micron scale. Therefore, signatures of mesoscopic CDW transport are expected to occur. Here, we discuss two observations that are related to the small volume of our structures.

At low temperatures, we observe strong hysteresis effects in the CDW current. As an example, two $I_{CDW}(V)$ curves with opposite sweep direction are shown in Fig. 5. In the pinned state, both $I(V)$ curves are smooth. In the sliding regime, however, the behavior depends on sweep direction. After a pinning-to-sliding transition, strong fluctuations of the CDW current are visible. If the $I(V)$ is measured in the opposite direction, however, the $I(V)$ is much smoother, and I_{CDW} is lower for the same voltage. Curves such as shown in Fig. 5 were measured for several temperatures and voltage probe spacings. The hysteresis effects are most pronounced for small voltage probe spacings, and increase with decreasing temperature. We suggest that the observed fluctuations of the CDW current are associated with metastable states. For the smallest spacings, the volume over which voltage is measured may consist of only a few coherent domains. A switching process in one of the domains will then cause a significant change of the CDW current.

For all voltage probe spacings, $I(V)$ curves measured in the transposed configuration (i.e., current and voltage probes are interchanged) are different from $I(V)$ curves measured in the standard four-terminal configuration. The dashed curve in Fig. 3 denotes a transposed curve for the 2 μm spaced contact at 130 K, where hysteresis effects are absent. As compared to the measurement in the standard four-terminal configuration, the same I_{CDW} corresponds to a higher voltage. The difference between the curves is generally interpreted in terms of a phase-slip voltage V_{PS} , required to condense normal electrons into the CDW and vice versa [10–12]. At length scales shorter than a few micron, we find that this V_{PS} is reduced, in agreement with [7]. More studies are needed to make this observation conclusive.

4. Conclusion

We have presented dc electrical transport data on lithographically patterned NbSe₃ wire structures with submicron dimensions. Measurements of the low-bias resistivity and the depinning field for CDW sliding show that the crystal quality has not degraded significantly in the pat-

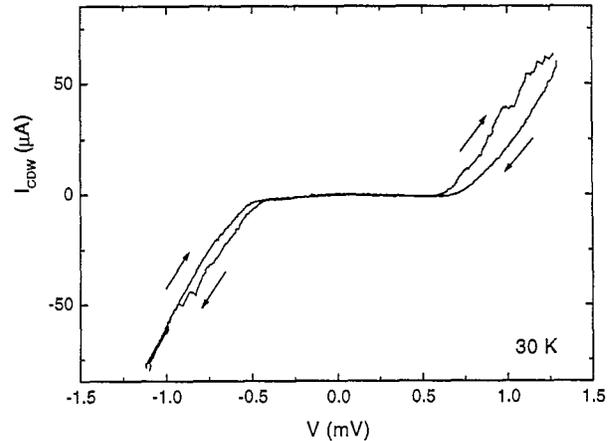


Figure 5: I_{CDW} versus voltage for the 2 μm spaced contacts on the 0.5 μm wide wire at 30 K. The arrows denote the sweep direction. Strong fluctuations and hysteresis in the CDW current are observed in the sliding regime of the $I(V)$.

terned process. Therefore, the structures are a good system for the study of mesoscopic CDW transport. Further measurements will look in more detail at fluctuation effects and phase-slip voltages. AC effects such as narrow-band noise and mode locking are to be explored in the mesoscopic regime.

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